Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (withdrawn). A method for producing a clock output signal, which comprises:

receiving an input signal that contains an information item representing a phase;

producing a plurality of clock signals having phases that are respectively shifted from one another by a predetermined amount;

weighting each one of the plurality of the clock signals in dependence on the information item that is contained in the input signal; and

mixing the weighted clock signals in order to produce a clock output signal having a phase that essentially matches the phase that is represented by the phase information item.

Claim 2 (withdrawn). The method according to claim 1, which comprises:

producing a clock input signal having a predetermined frequency and a phase;

producing the plurality of the clock signals by shifting the phase of the clock input signal by an amount that is selected from the group consisting of the predetermined amount and a multiple of the predetermined amount; and

producing the plurality of the clock signals so that each of the plurality of the clock signals has the predetermined frequency.

Claim 3 (withdrawn). The method according to claim 2, wherein the plurality of the clock signals that are produced are four clock signals whose phases are shifted from one another by 90°.

Claim 4 (withdrawn). The method according to claim 3, which comprises using a quadrature oscillator to produce the four clock signals from the clock input signal.

Claim 5 (withdrawn). The method according to claim 1, which comprises performing the step of mixing the weighted clock signals by adding the weighted clock signals.

Claim 6 (withdrawn). The method according to claim 1, which comprises, when mixing the weighted clock signals, performing band-limiting to filter out harmonics.

Claim 7 (withdrawn). An apparatus for producing a clock output signal, comprising:

an input for receiving an input signal containing a phase information item representing a phase;

a clock generator for producing a plurality of clock signals having phases that are shifted from one another by a predetermined amount; and

a weighting and mixing circuit for weighting each one of the plurality of the clock signals based on the phase information item to obtain a plurality of weighted clock signals;

said weighting and mixing circuit also for mixing the plurality of the weighted clock signals to produce a clock output signal having a phase that essentially matches the phase represented by the phase information item.

Claim 8 (withdrawn). The apparatus according to claim 7, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay lock loop control loop including said input, said clock generator, and said weighting and mixing circuit.

Claim 9 (withdrawn). The apparatus according to claim 8, wherein said clock generator is formed by a quadrature oscillator producing four clock signals having phases that are shifted from one another by 90°; the four clock signals defining the plurality of the clock signals.

Claim 10 (withdrawn). The apparatus according to claim 7, wherein said clock generator is formed by a quadrature oscillator producing four clock signals having phases that are shifted from one another by 90°; the four clock signals defining the plurality of the clock signals.

Claim 11 (currently amended). A control loop, comprising:

a phase shifter for producing an output with a first clock phase;

a phase detector for detecting a phase difference between a second clock phase of a data signal and the first clock phase,

said phase detector producing an output signal based on the detected phase difference;

a charge pump for integrating the output signal of said phase detector, said charge pump producing a ~~regulation signal~~ control voltage for said phase shifter; and

said phase shifter changing over a phase regulation direction ~~at predetermined switching points based on said regulation signal~~ when the control voltage reaches an upper or a lower range limit thereof;

said changing over of said phase regulation direction being performed with a hysteresis behavior.

Claim 12 (previously presented). The control loop according to claim 11, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay locked loop control loop including said phase shifter, said phase detector, and said charge pump.

Claim 13 (currently amended). A method for producing a clock signal, which comprises:

detecting a phase difference between a clock phase of a first input signal and a clock phase of a first output signal of ~~the~~ a phase shifter;

producing a second output signal based on the detected phase difference;

producing a ~~second input signal~~ control voltage for the phase shifter by integrating the second output signal; and

changing a phase regulation direction of the phase shifter ~~at predetermined switching points based on the second input signal~~ when the control voltage reaches an upper or a lower range limit thereof, the changing over of the phase regulation direction being performed with a hysteresis behavior.

Claim 14 (currently amended). A phase shifter for producing an output signal, which comprises:

a circuit for receiving an input signal having a phase and for receiving a control voltage within a voltage range;

said circuit ~~also~~ being configured for producing an output signal having a phase , the phase of the output signal being controlled by the control voltage;

said circuit ~~designed~~ being configured for changing a phase regulation direction of the phase shifter when the control voltage reaches an upper or a lower range limit thereof;

~~at predetermined switching points based on an input signal,~~ ~~the~~ wherein the changing over of the phase regulation direction ~~being~~ is performed with a hysteresis behavior.

Claims 15-17 (canceled).